

JEDEC STANDARD

DDR5 Small Outline Dual Inline Memory Module (SODIMM) Common Standard

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DDR5 SMALL OUTLINE DUAL INLINE MEMORY MODULE (SODIMM) COMMON STANDARD

From JEDEC Board Ballot JCB-21-54, formulated under the cognizance of the JC-45.3 Subcommittee on Unbuffered DRAM Modules, item number 2262.06B.

1 Scope

This standard defines the electrical and mechanical requirements for 262-pin, 1.1 V (VDD), Small Outline, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR5 SDRAM SODIMMs). These DDR5 SODIMMs are intended for use as main memory when installed in Computers, laptops and other systems.

Reference design examples are included which provide an initial basis for DDR5 SODIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC5-4000, PC5-4800, and beyond. All DDR5 SODIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

2 Related Standards

- JESD79-5: DDR5 SDRAM Standard
- JESD300-5: SPD5118 Hub and Serial Presence Detect Device Standard
- JESD301-2: PMIC5100 Power Management Integrated Circuit (PMIC) Device Standard
- JESD400-5: DDR5 Serial Presence Detect (SPD) Contents
- JESD401-5: DDR5 DIMM Label
- JESD403-1: JEDEC Module Sideband Bus
- MO-210: Plastic Bottom Grid Array, 0.80 mm Pitch, Rectangular Family Package
- MO-337: 262 PIN SODIMM, 0.50 mm Pitch Package

3 Product Family Attributes

Table 1 —Product Family Attributes

DIMM Organization	x64 (x32, 2 channels), x72 ECC (x36, 2 channels)	
DIMM Dimensions (nominal)	69.6 mm x 30.0 mm	MO-337 Same width as DDR4, but 2 more pins.
Pin Count and Pitch	262 on 0.5 mm centers	
DDR5 SDRAMs Supported	16 Gb, 24 Gb, 32 Gb, 64 Gb	MO-210
Capacity	16 GB - 128 GB	
DDR5 SDRAM width	x8, x16	
Serial Presence Detect with Thermal Sensor	1024 byte	JESD300-5
PMIC	PMIC5100	JESD301-2
Voltage Options	5 V (VIN_BULK)	
Interface	1.1 V signaling	

4 Environmental Requirements

DDR5 SODIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation. These will typically be non-ECC SODIMMs.

DDR5 SODIMMs that have ECC support are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Table 2 — Environmental Parameters (Example)

Symbol	Parameter	Rating	Units	
TOPR	DRAM Operating Temperature	0 to +95	°C	
TSTG	Storage Temperature	-55 to +100	°C	
<p>NOTE 1 Operating temperature applies to the case temperature of all SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs are at the minimum and maximum values. See JESD402-1 for details.</p> <p>NOTE 2 Storage temperature applies to the case temperature of all components on the module. See JESD402-1 for details. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.</p>				

5 Connector Pinout and Signal Description

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command/Address bus	HSCL	SidebandBus clock
CS0_A_n, CS1_A_n, CS0_B_n, CS1_B_n	SDRAM Chip Select	HSDA	SidebandBus data
DQ0_A – DQ31_A, DQ0_B – DQ31_B	DIMM memory data bus	HSA	SidebandBus address
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits	ALERT_n	SDRAM ALERT_n
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set DRAMs to a known State
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)	VIN_BULK	5 V power input supply to the PMIC for analog circuits
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks	VSS	Power supply return (ground)
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)	PWR_GOOD	Power good indicator
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)	PWR_EN	PMIC Enable
		RFU	Reserved for future use
NOTE 1 DDR5 SODIMM has 2 channels (channel-A and channel-B) of signal bus. The signals with suffix: _A (e.g., DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B.			

5 Connector Pinout and Signal Description (cont'd)

Table 4 — Input/Output Functional Description

Symbol	Type	I/O Level	Function
CK0_A_t, CK0_A_c, CK1_A_t, CK1_A_c, CK0_B_t, CK0_B_c, CK1_B_t, CK1_B_c	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA12_A, CA0_B - CA12_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS0_A_n - CS1_A_n, CS0_B_n - CS1_B_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input/Output	VDDQ	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A - CB3_A, CB0_B - CB3_B	Input/Output	VDDQ	DIMM ECC check bits
DQS0_A_t - DQS4_A_t, DQS0_A_c - DQS4_A_c, DQS0_B_t - DQS4_B_t, DQS0_B_c - DQS4_B_c	Input/Output	VDDQ	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n - DM3_A_n, DM0_B_n - DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1.
ALERT_n	Input/Output	VDD	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.

Table 4 — Input/Output Functional Description (cont'd)

Symbol	Type	I/O Level	Function
HSCL	Input	1.0 V	Host SidebandBus bus clock, supplied by the controller.
HSDA	Input / Output	1.0 V	Host SidebandBus data, connected from the controller to Hub or Host bus Target devices.
HSA	Input	2.1 V max	Host SidebandBus bus device ID address pin; input to a Hub or other client device to distinguish between identical devices in the I3C-Basic/I2C address range.
RFU			Reserved for Future Use. No on DIMM electrical connection is present.
PWR_GOOD	Input / Output	Open Drain	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceed the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
PWR_EN	Input	3.3 V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin.
VIN_BULK	Supply	5 V	5 V power input supply to the PMIC for analog circuits.
VSS	Supply		Ground

5.1 DDR5 SODIMM Connector Pin Assignments

Table 5 — DDR5 SODIMM 262 Pin Connector Pin Wiring Assignments

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	VIN_BULK	2	HSA	131	CK0_A_t	132	CK1_A_t
3	VIN_BULK	4	HSCL	133	CK0_A_c	134	CK1_A_c
5	RFU	6	HSDA	135	VSS	136	VSS
7	PWR_GOOD	8	PWR_EN	137	CK0_B_t	138	CK1_B_t
9	VSS	10	VSS	139	CK0_B_c	140	CK1_B_c
11	DQ0_A	12	DQ1_A	141	VSS	142	VSS
13	VSS	14	VSS	143	RFU	144	CA12_B
15	DQ2_A	16	DQ3_A	145	CA11_B	146	CA10_B
17	VSS	18	VSS	147	VSS	148	VSS
19	DM0_A_n	20	DQS0_A_c	149	CA9_B	150	CA8_B

Table 5 — DDR5 SODIMM 262 Pin Connector Pin Wiring Assignments (cont'd)

21	VSS	22	DQS0_A_t	151	CA7_B	152	CA6_B
23	DQ4_A	24	VSS	153	VSS	154	VSS
25	VSS	26	DQ5_A	155	CA5_B	156	CA4_B
27	DQ6_A	28	VSS	157	CA3_B	158	CA2_B
29	VSS	30	DQ7_A	159	VSS	160	VSS
31	DQ8_A	32	VSS	161	CS0_B_n	162	CA1_B
33	VSS	34	DQ09_A	163	RESET_n	164	CA0_B
35	DQ10_A	36	VSS	165	CS1_B_n	166	VSS
37	VSS	38	DQ11_A	167	VSS	168	CB0_B
39	DQS1_A_c	40	VSS	169	DQS4_B_c	170	VSS
41	DQS1_A_t	42	DM1_A_n	171	DQS4_B_t	172	CB1_B
43	VSS	44	VSS	173	VSS	174	VSS
45	DQ12_A	46	DQ13_A	175	CB3_B	176	CB2_B
47	VSS	48	VSS	177	VSS	178	VSS
49	DQ14_A	50	DQ15_A	179	DQ0_B	180	DQ1_B
51	VSS	52	VSS	181	VSS	182	VSS
53	DQ16_A	54	DQ17_A	183	DQ2_B	184	DQ3_B
55	VSS	56	VSS	185	VSS	186	VSS
57	DQ18_A	58	DQ19_A	187	DM0_B_n	188	DQS0_B_c
59	VSS	60	VSS	189	VSS	190	DQS0_B_t
61	DM2_A_n	62	DQS2_A_c	191	DQ4_B	192	VSS
63	VSS	64	DQS2_A_t	193	VSS	194	DQ5_B
65	DQ20_A	66	VSS	195	DQ6_B	196	VSS
67	VSS	68	DQ21_A	197	VSS	198	DQ7_B
69	DQ22_A	70	VSS	199	DQ8_B	200	VSS
71	VSS	72	DQ23_A	201	VSS	202	DQ9_B
73	DQ24_A	74	VSS	203	DQ10_B	204	VSS
75	VSS	76	DQ25_A	205	VSS	206	DQ11_B
77	DQ26_A	78	VSS	207	DQS1_B_c	208	VSS
79	VSS	80	DQ27_A	209	DQS1_B_t	210	DM1_B_n
81	DQS3_A_c	82	VSS	211	VSS	212	VSS
83	DQS3_A_t	84	DM3_A_n	213	DQ12_B	214	DQ13_B
85	VSS	86	VSS	215	VSS	216	VSS
87	DQ28_A	88	DQ29_A	217	DQ14_B	218	DQ15_B
89	VSS	90	VSS	219	VSS	220	VSS
91	DQ30_A	92	DQ31_A	221	DQ16_B	222	DQ17_B
93	VSS	94	VSS	223	VSS	224	VSS
95	CB0_A	96	CB1_A	225	DQ18_B	226	DQ19_B
97	VSS	98	VSS	227	VSS	228	VSS
99	CB2_A	100	DQS4_A_c	229	DM2_B_n	230	DQS2_B_c

Table 5 — DDR5 SODIMM 262 Pin Connector Pin Wiring Assignments (cont'd)

101	VSS	102	DQS4_A_t	231	VSS	232	DQS2_B_t
103	CB3_A	104	VSS	233	DQ20_B	234	VSS
105	VSS	106	CS0_A_n	235	VSS	236	DQ21_B
107	CA0_A	108	ALERT_n	237	DQ22_B	238	VSS
109	CA1_A	110	CS1_A_n	239	VSS	240	DQ23_B
111	VSS	112	VSS	241	DQ24_B	242	VSS
113	CA2_A	114	CA3_A	243	VSS	244	DQ25_B
115	CA4_A	116	CA5_A	245	DQ26_B	246	VSS
117	VSS	118	VSS	247	VSS	248	DQ27_B
119	CA6_A	120	CA7_A	249	DQS3_B_c	250	VSS
121	CA8_A	122	CA9_A	251	DQS3_B_t	252	DM3_B_n
123	VSS	124	VSS	253	VSS	254	VSS
125	CA10_A	126	CA11_A	255	DQ28_B	256	DQ29_B
KEY				257	VSS	258	VSS
127	CA12_A	128	RFU	259	DQ30_B	260	DQ31_B
129	VSS	130	VSS	261	VSS	262	VSS

6 Power Details

6.1 DIMM Voltage Requirements

Please refer to the latest version of JESD301-2: PMIC5100 Power Management IC Standard for details and updates.

The following is general information for DDR5 SODIMM:

- The DDR5 SODIMM has a PMIC on the PCB. All required voltages are generated by the PMIC from the VIN_BULK supply.
- The DDR5 SODIMM uses the PMIC in Single Phase Regulator mode. Typically, one of the SWA or SWB output is used for VDD, and the other output is used for VDDQ.
- GSI_n pin must be connected to VSS on the DIMM.

6.2 Soft Stop Time Programing for the PMIC Registers

To reduce the power line spike, the Soft Stop Time register setting for all PMIC output switch rails on module must be set to 0b11.

6.2 Soft Stop Time Programing for the PMIC Registers (cont'd)

Table 6 — PMIC Register setting for the Soft Stop

PMIC Register	Description	Register Bit	Value (Binary)	Soft Stop Time (ms)
0x46	R46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME	[1:0]	11	4
0x4A	R4A [1:0]: SWB_OUTPUT_SOFT_STOP_TIME	[1:0]	11	4
0x4C	R4C [1:0]: SWC_OUTPUT_SOFT_STOP_TIME	[1:0]	11	8

7 Component Details

7.1 Component Types and Placement

Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for DDR5 SDRAM signals. Decoupling capacitors for DDR5 SDRAM devices must be located near the device power pins.

Table 7 — DDR5 x8 SDRAM Pad Array

	1	2	3	4	5	6	7	8	9	
A	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	A
B	VDD	VDDQ	DQ2				DQ3	VDDQ	VDD	B
C	VSS	DQ0	DQS_t				DM_n, TDQS_t	DQ1	VSS	C
D	VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ	D
E	VDD	DQ4	DQ6				DQ7	DQ5	VDD	E
F	VSS	VDDQ	VSS				VSS	VDDQ	VSS	F
G	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	G
H	ALERT_n	VSS	CS_n				CK_c	VSS	VDD	H
J	VDDQ	CA4	CA0				CA1	CA5	VDDQ	J
K	VDD	CA6	CA2				CA3	CA7	VDD	K
L	VDDQ	VSS	CA8				CA9	VSS	VDDQ	L
M	CAI	CA10	CA12				CA13	CA11	RESET_n	M
N	VDD	VSS	VDD				VPP	VSS	VDD	N

DDR5 SODIMM reference design uses the pad array with support balls.

Table 7 — DDR5 x8 SDRAM Pad Array (cont'd)

MO-210-AL (x8)										MO-210-AN (x8) with support balls											
	1	2	3	4	5	6	7	8	9		1	2	3	4	5	6	7	8	9	10	11
A	○	○	○	+	+	+	○	○	○	A	○	○	○	+	+	+	○	○	○	○	○
B	○	○	○	+	+	+	○	○	○	B	+	○	○	○	+	+	+	○	○	○	+
C	○	○	○	+	+	+	○	○	○	C	+	○	○	○	+	+	+	○	○	○	+
D	○	○	○	+	+	+	○	○	○	D	+	○	○	○	+	+	+	○	○	○	+
E	○	○	○	+	+	+	○	○	○	E	+	○	○	○	+	+	+	○	○	○	+
F	○	○	○	+	+	+	○	○	○	F	+	○	○	○	+	+	+	○	○	○	+
G	○	○	○	+	+	+	○	○	○	G	+	○	○	○	+	+	+	○	○	○	+
H	○	○	○	+	+	+	○	○	○	H	+	○	○	○	+	+	+	○	○	○	+
J	○	○	○	+	+	+	○	○	○	J	+	○	○	○	+	+	+	○	○	○	+
K	○	○	○	+	+	+	○	○	○	K	+	○	○	○	+	+	+	○	○	○	+
L	○	○	○	+	+	+	○	○	○	L	+	○	○	○	+	+	+	○	○	○	+
M	○	○	○	+	+	+	○	○	○	M	+	○	○	○	+	+	+	○	○	○	+
N	○	○	○	+	+	+	○	○	○	N	○	○	○	○	+	+	+	○	○	○	○

○ Populated ball
+ Ball not populated

NOTE 1 Additional columns and rows of inactive balls in MO-210 Terminal Pattern AU(x16) with support balls are for mechanical support only and should not be tied to either electrically high or low.

NOTE 2 Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.

NOTE 3 Please refer to the latest version of JESD79-5: DDR5 SDRAM Standard for updates.

Table 8 — DDR5 x16 SDRAM Pad Array

	1	2	3	4	5	6	7	8	9	
A	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	A
B	VDD	VDDQ	DQU2				DQU3	VDDQ	VDD	B
C	VSS	DQU0	DQSU_t				DMU_n	DQU1	VSS	C
D	VDDQ	VSS	DQSU_c				RFU	VSS	VDDQ	D
E	VDD	DQU4	DQU6				DQU7	DQU5	VDD	E
F	VDD	VDDQ	DQL2				DQL3	VDDQ	VDD	F
G	VSS	DQL0	DQSL_t				DML_n	DQL1	VSS	G
H	VDDQ	VSS	DQSL_c				RFU	VSS	VDDQ	H
J	VDD	DQL4	DQL6				DQL7	DQL5	VDD	J
K	VSS	VDDQ	VSS				VSS	VDDQ	VSS	K
L	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	L
M	ALERT_n	VSS	CS_n				CK_c	VSS	VDD	M
N	VDDQ	CA4	CA0				CA1	CA5	VDDQ	N
P	VDD	CA6	CA2				CA3	CA7	VDD	P
R	VDDQ	VSS	CA8				CA9	VSS	VDDQ	R
T	CAI	CA10	CA12				CA13	CA11	RESET_n	T
U	VDD	VSS	VDD				VPP	VSS	VDD	U

DDR5 SODIMM reference design uses the pad array with support balls.

Table 8 — DDR5 x16 SDRAM Pad Array (cont'd)

MO-210-AT (x16)										MO-210-AU (x16) with support balls												
	1	2	3	4	5	6	7	8	9		1	2	3	4	5	6	7	8	9	10	11	
A	○	○	○	+	+	+	+	○	○	A	○	○	○	○	+	+	+	+	○	○	○	○
B	○	○	○	+	+	+	+	○	○	B	+	○	○	○	+	+	+	+	○	○	○	+
C	○	○	○	+	+	+	+	○	○	C	+	○	○	○	+	+	+	+	○	○	○	+
D	○	○	○	+	+	+	+	○	○	D	+	○	○	○	+	+	+	+	○	○	○	+
E	○	○	○	+	+	+	+	○	○	E	+	○	○	○	+	+	+	+	○	○	○	+
F	○	○	○	+	+	+	+	○	○	F	+	○	○	○	+	+	+	+	○	○	○	+
G	○	○	○	+	+	+	+	○	○	G	+	○	○	○	+	+	+	+	○	○	○	+
H	○	○	○	+	+	+	+	○	○	H	+	○	○	○	+	+	+	+	○	○	○	+
J	○	○	○	+	+	+	+	○	○	J	+	○	○	○	+	+	+	+	○	○	○	+
K	○	○	○	+	+	+	+	○	○	K	+	○	○	○	+	+	+	+	○	○	○	+
L	○	○	○	+	+	+	+	○	○	L	+	○	○	○	+	+	+	+	○	○	○	+
M	○	○	○	+	+	+	+	○	○	M	+	○	○	○	+	+	+	+	○	○	○	+
N	○	○	○	+	+	+	+	○	○	N	+	○	○	○	+	+	+	+	○	○	○	+
P	○	○	○	+	+	+	+	○	○	P	+	○	○	○	+	+	+	+	○	○	○	+
R	○	○	○	+	+	+	+	○	○	R	+	○	○	○	+	+	+	+	○	○	○	+
T	○	○	○	+	+	+	+	○	○	T	+	○	○	○	+	+	+	+	○	○	○	+
U	○	○	○	+	+	+	+	○	○	U	○	○	○	○	+	+	+	+	○	○	○	○

○ Populated ball

+ Ball not populated

NOTE 1 Additional columns and rows of inactive balls in MO-210 Terminal Pattern AU(x16) with support balls are for mechanical support only and should not be tied to either electrically high or low.

NOTE 2 Some of the additional support balls can be selectively populated under the supplier’s discretion. Refer to supplier’s datasheet.

NOTE 3 Please refer to the latest version of JESD79-5: DDR5 SDRAM Standard for updates.

7.2 Decoupling Guidelines

Table 9 — Decoupling Capacitor Guidelines

	Guideline	Note
VDD	Minimum of two decoupling capacitors to VSS per SDRAM	Should be placed as close as possible to the DRAM VDD ball
VDDQ	Minimum of two decoupling capacitors to VSS per SDRAM	Should be placed as close as possible to the DRAM VDDQ ball
VPP	Minimum of one decoupling cap per DRAM VPP pin	Should be placed as close as possible to the DRAM VPP ball
VIN_BULK	Near the Gold Finger : 4.7 μ F, 0402, 10 V, 1 piece	
	Near the PMIC IC : Refer to the PMIC specification	

NOTE 1 Decoupling capacitor values for VDD, VDDQ and VPP vary by module and may be staggered to achieve best overall impedance vs. frequency response.

NOTE 2 Recommended values for decoupling for VDD, VDDQ, and VPP are 1 μ F, 2.2 μ F, 4.7 μ F, and 10 μ F.

NOTE 3 Depending on the DRAM package size, all placements may not be possible.

8 DIMM Design Details

8.1 Signal Groups

This standard categorizes DDR5 SDRAM timing-critical signals into four groups. The following summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. There are two channels of signal groups. Left side is channel-A, and Right side is channel-B.

Signal Groups:

1. Clock (CK or CLK)
2. Command/Address (CMD/ADR)
3. Chip Select (CS)
4. Data Bus (including ECC byte) (DQ, Strobe)

8.2 Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for SODIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. A typical data net structure is shown in Figure 1.

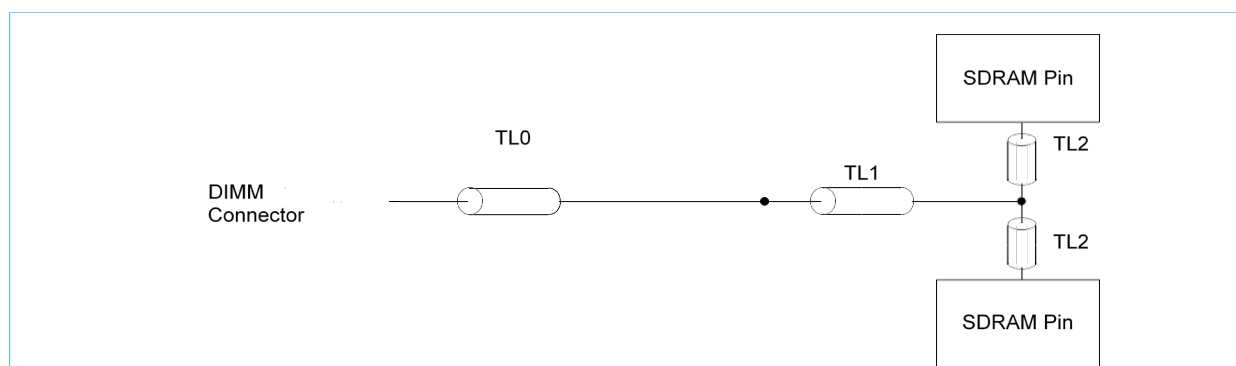


Figure 1 — Net Structure Example for Two Rank DIMM

8.3 General Net Structure Routing Rules

Net structure diagrams for each signal group are shown in the following clauses. The remainder of this clause provides a general overview of DDR5 net structure concepts and documents the routing rules to be followed in the design of the DDR5 modules.

To use simulation almost exclusively, some conditions must be defined so that the same conclusion is reached using different simulation tools. See Table 10 for an example.

Table 10 — Simulation Conditions Example

Group	Parameter	Condition
Data Bus	Motherboard Length	100 mm
	Motherboard Impedance	35 Ω (68 Ω differential for Strokes)
	Motherboard Configuration	One DIMM slot
	Routing Type	Stripline (Micro-strip)
	Driver	34 Ω DRAM with DRAM package
Command/Address, Chip Select	Motherboard Length	100 mm
	Motherboard Impedance	50 Ω (single ended)
	Motherboard Configuration	One DIMM per channel
	Driver	34 Ω DRAM with DRAM package
Clock	Motherboard Length	100 mm
	Motherboard Impedance	50 Ω differential
	Motherboard Configuration	One DIMM per channel
	Driver	34 Ω DRAM with DRAM package

8.3.1 CK, CMD/ADR, and CS Groups

The DDR5 modules implement a fly-by topology for routing CK, Command/Address, and chip select signal groups. The Command/Address and Chip Select groups on DDR5 modules are length/delay matched to CK, between the connector and each SDRAM. Table provides a summary of the length/delay matching rules associated the CK, Command/Address and chip select groups.

For the length tables in the Annexes where there is not a specified tolerance and the tolerance is not covered by Table 11, a value of ± 1.0 mm shall be used.

8.3.1 CK, CMD/ADR and CS Groups (cont'd)

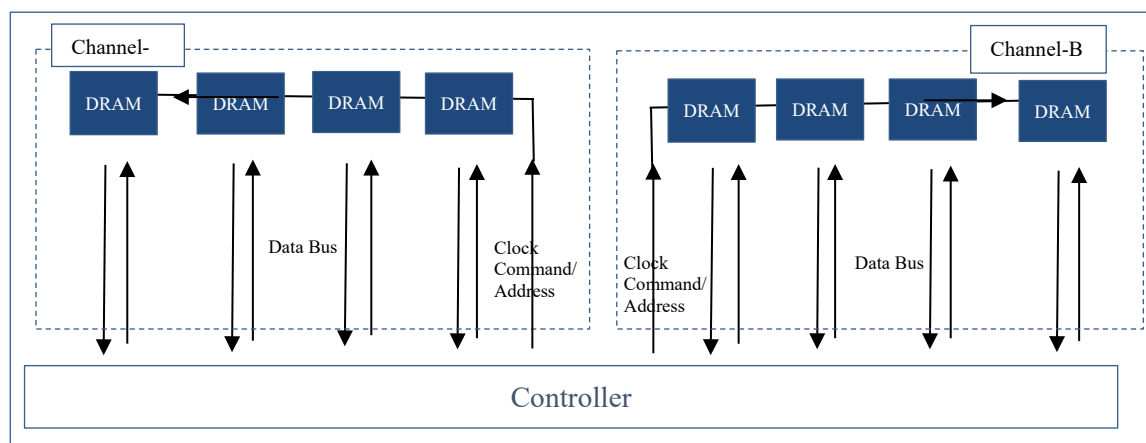


Figure 2 — Fly By Topology Example

Table 11 — CK, CMD/ADR, and CS Group Length Matching Rules

Signal Group	Matching Rules
CK trace length	CK trace length should be as short as possible to reduce jitter, but still need to consider the relationship with Command/Address by simulation at each DRAM.
CK_t-to-CK_c Matching	Match TLx segment by TLx segment to within 0.1 mm. See Figure 4 for naming.
CK Pair-to-CK Pair Matching (Pair- to-Pair: Average Length)	Match total compensated length from connector to each SDRAM to within 0.5 mm
Command/Address Matching	Match total compensated length from connector to each SDRAM to within 0.2 mm
Chip Select Matching	Match total compensated length from connector to each SDRAM to within 0.2 mm
Command/Address Channel_A/B Matching	Match total compensated lengths of channel A and B within 0.3 mm.
Chip Select Channel_A/B Matching	Match total compensated lengths of channel A and B within 0.3 mm.
TL2 MAX Stub Length Limits	$TL2 \leq 3.0$ mm. See Figure 3 for naming. (Recommend placing the breakout via under DRAM at the center of 4 DRAM balls and keep $TL2 = 0.6$ mm)
CK First-to-Last Length	Maximum length from first SDRAM and last SDRAM is 90 mm.
Neckdown Length	Determined by simulation.
NOTE 1 All length matching is done using velocity compensated stripline equivalent lengths. NOTE 2 A velocity compensation ratio of 1.1 will be used ($MS\ length/1.1 = SL\ equivalent\ length$). NOTE 3 Neckdown length is the trailing portion of the TL1 segment into via under the first DRAM of daisy-chain. NOTE 4 Maximum first-to-last length can be calculated by subtracting length to first SDRAM from length to last SDRAM.	

8.3.2 Lead-in versus Loaded Sections

See Figure 3 for transmission line name designations. The CK, CMD/ADR, and CS topologies are conceptually divided into two topology sections. The segments between the connector and the first SDRAM node via (TL0 + TL1) are collectively termed the lead-in section, while the segments that run between SDRAM node vias (TL3), as well as the SDRAM load stubs (TL2), are collectively termed the loaded section.

In order to reduce the impedance discontinuity seen at the first load, the lead-in section is routed at a lower nominal impedance than the loaded section, although some modules may vary. The transition from the wider lead-in trace width to the standard width of the loaded section must occur within a length window preceding the first SDRAM node via, which is termed the neck down length.

The two different impedance sections at lead-in may not be required for example for the modules which have short TL0+TL1 length (e.g., less than 25 mm). This should be determined by simulation.

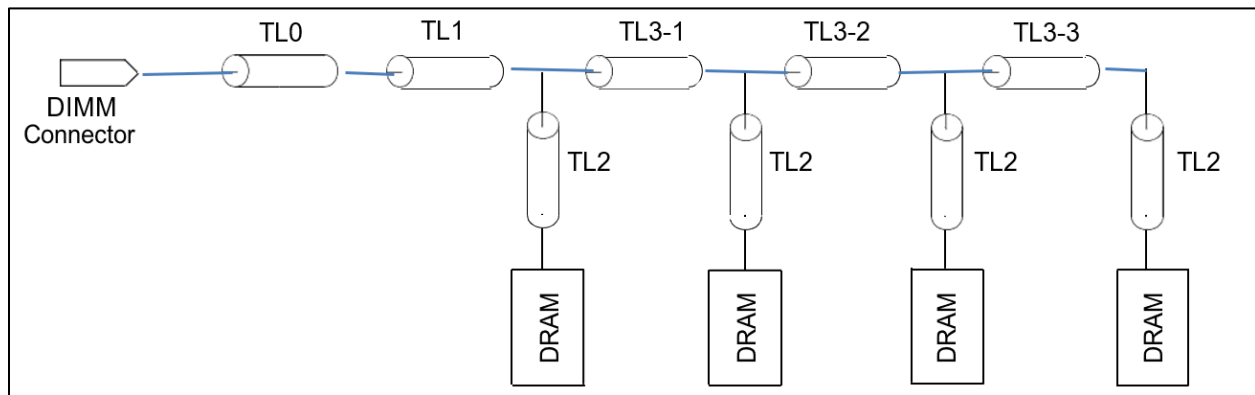


Figure 3 — Command/Address Routing Topology Example

8.3.3 Length/Delay Matching to SDRAM Devices

As mentioned previously, length/delay matching is required between the connector and each SDRAM individually. The length/delay matching process is iterative in nature, and there is no single-best method defined. It is generally recommended that the path from the connector to the first SDRAM (TL0 + TL1) be matched across the CK group, and then across the CTRL and ADD/CMD groups—as per the length matching guidelines — adjusting the CK length as needed to reach the length window of the CTRL and ADD/CMD groups. For the DDR5 SODIMM, usually the breakout via from the DRAM pin is located between 4 DRAM pins and lengths are all 0.6 mm, in that case TL2 does not need to be included in the length calculation.

Once length/delay matching to the first device is complete, the length matching to the remaining devices is straightforward and can be accomplished by simply length-matching the intra-node segments (TL3-x), assuming the TL2 stub length for a given signal does not vary from SDRAM to SDRAM.

The total compensated length from the connector to the first and last SDRAM is documented in the segment length tables for each module type, in the net structure definitions clauses; however, it is assumed that the length matching rules are met at all SDRAM devices.

8.3.4 Velocity Compensation

Since the lead-in section can have a wide variation in the proportion of its length routed as microstrip (MS) and stripline (SL), the length/delay matching process includes a mechanism for compensating for the velocity delta between these two types of PCB interconnects. A compensation factor of 1.1 has been specified for this purpose. All microstrip segment lengths are to be divided by 1.1 before summation into the length matching equation. The resulting compensated length is termed the stripline equivalent length. While some amount of residual velocity mismatch skew remains in the design, the process is a substantial improvement over simple length matching.

8.3.5 Load/Delay Compensation

The concept of load/delay compensation refers to the technique whereby the segment lengths between SDRAMs, on the CLK and CS signal groups, are purposely lengthened in order to add additional flight time delay, as required to compensate for the fact that the CMD/ADR topology for 2 rank modules has 2 loads (1 top + 1 bottom) for each fly-by node, whereas the CLK and CS topologies have only one load per node. Where implemented, the CLK and CS segments between SDRAMs shall be routed longer than the corresponding segment on CMD/ADR group. A specific number can be identified using simulation or calculation. The net result of this compensation is less overall CMD/ADR to CLK skew across the module, thereby improving the ability of the controller to correctly center the CLK within the CMD/ADR valid window at each SDRAM.

8.3.6 Data and Strobe Group

The DDR5 modules treat each byte lane as a separate signal sub-group, with each byte lane group length/delay matched with velocity compensation as previously described. The length of the individual byte lanes may vary substantially across the module, with the controller providing timing realignment circuitry.

A summary table of the length/delay matching rules associated with the data signal group is provided in Table 12.

8.3.6 Data and Strobe Group (cont'd)

Table 12 — Data and Strobe Group Length Matching Rules

Signal Group	Matching Rules
DQS _t -to-DQS _c Matching	Match TLx segment by TLx segment to within 0.1 mm
DQ to DQ and DM within a byte (x8/x16)	Match total compensated length from the connector to each SDRAM of DQ and DM signals within ± 0.5 mm
DQ/DM to DQS within Byte Lane	DQS length shall be as close as possible to DQ and DM lengths, and shall not be longer than DQ and DM.
Minimum Byte Lane Length (DQ, DQS, DM)	Minimum compensated length from the connector to the SDRAM shall not be less than 9.0 mm.
Maximum Byte Lane Length (DQ, DQS, DM)	Maximum compensated length from the connector to the SDRAM shall not be greater than 28.0 mm
NOTE 1 All length matching is done using velocity compensated stripline equivalent lengths and Via compensation. NOTE 2 A velocity compensation ratio of 1.1 will be used (MS length/1.1 = SL equivalent length). NOTE 3 For via equivalent length see the clause on Via compensation.	

8.3.7 ALERT_n Wiring

See Figure 4. Wiring example for the ALERT_n signal. DDR5 SODIMM has 2 channels of signal groups, but there is only one ALERT_n. Unlike DDR4 there is no direction restriction to the clock. The connection order can be the same as clock, or can be reverse order of clock. It requires a termination resistor at the far end from the card edge.

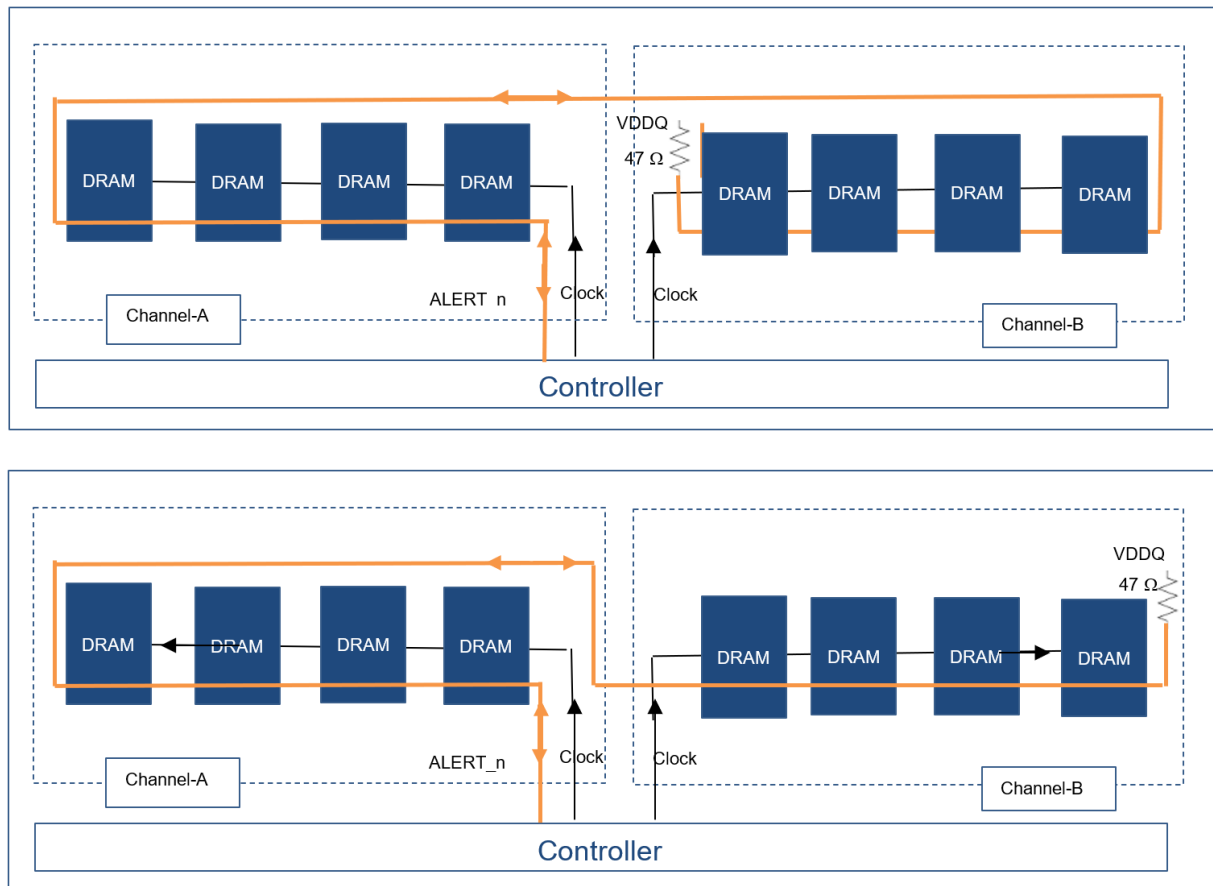


Figure 4 — ALERT_n Wiring Examples

8.3.8 RESET_n Wiring

See Figure 5 for wiring example for the RESET_n signal. The topology should be a daisy chain. There is no restriction for the connection ordering.

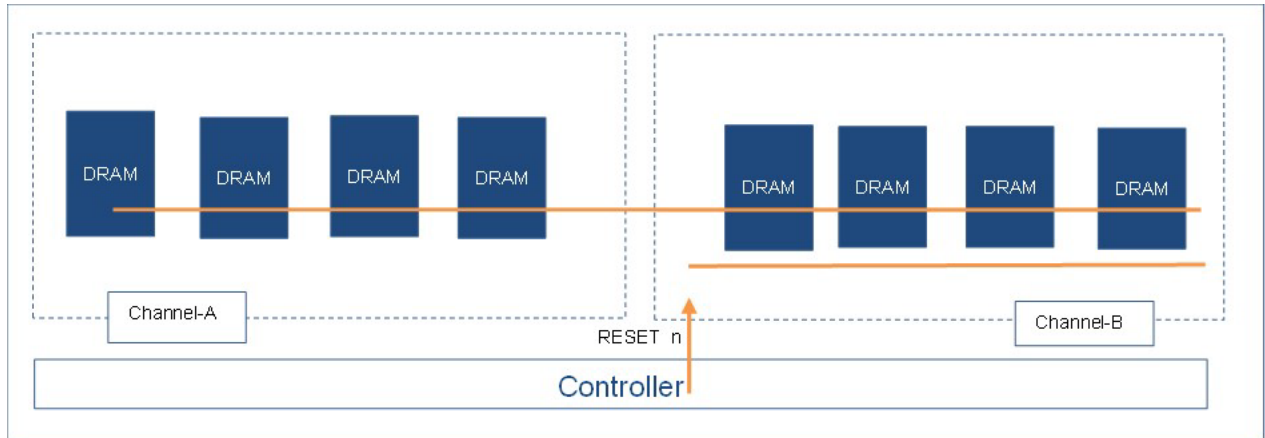


Figure 5 — RESET_n Wiring Example

8.3.9 Via Compensation

The JEDEC DDR5 SODIMM reference designs just adds the vertical length that the signal travels along the via barrel to the length calculation.

For the DRAMs which share a via (2 rank module case), the via barrel lengths to the top and bottom DRAMs are different. In that case the via barrel lengths are not included in the length calculation. Please see the length file which is zipped with the reference design.

8.3.9 Via Compensation (cont'd)

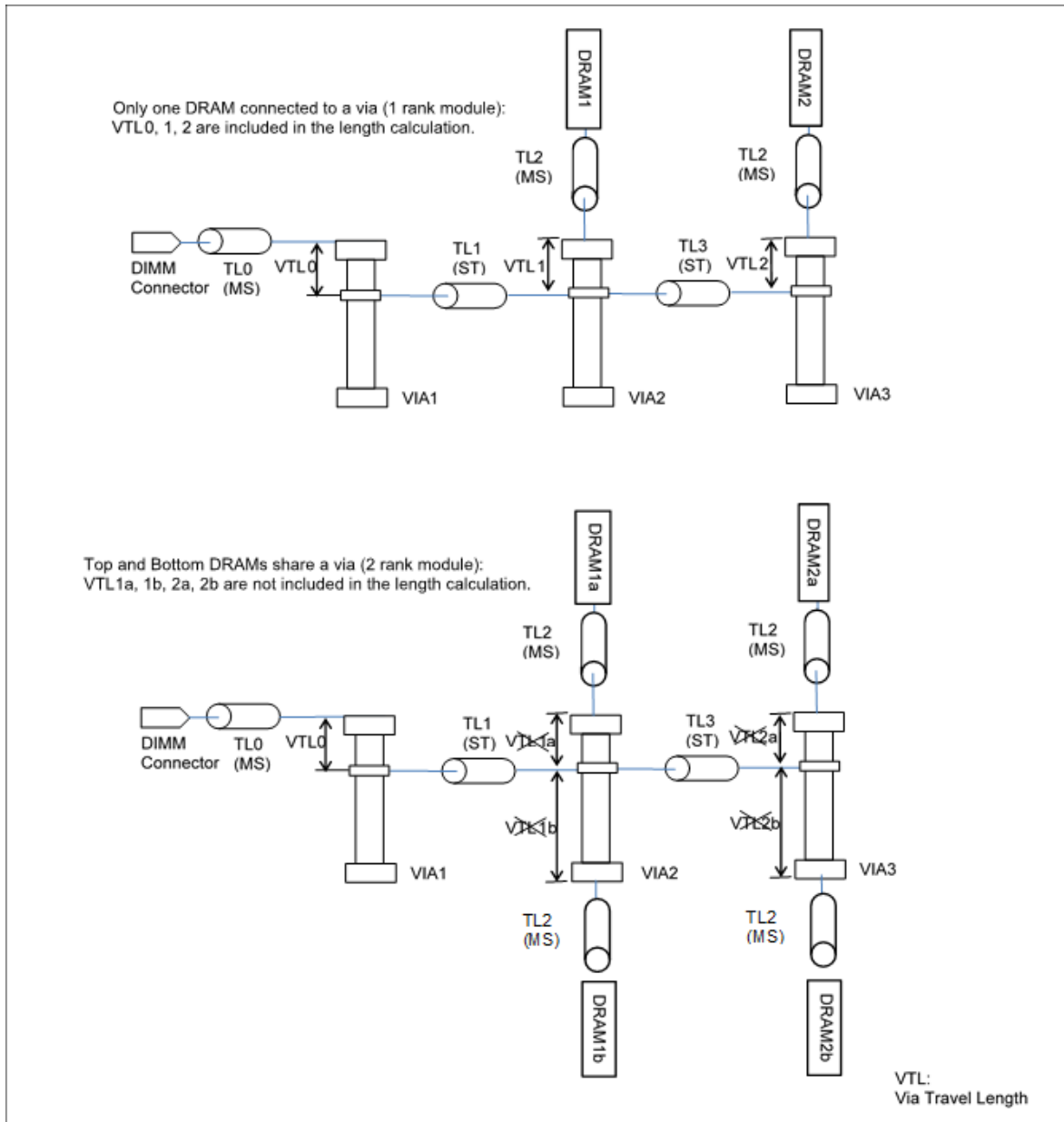


Figure 6 — Via Compensation Explanation

8.3.10 Plane Referencing

Table 13 — Plane Referencing

Signals	Reference	Notes
DQ, DQS, DM	Ground	
Command/Address	Ground	
Chip Select	Ground	
Clock	Ground	
SidebandBus	Ground	

8.4 Address Mirroring

DDR5 SDRAM has MIR input pin. This pin is connected to VSS or VDDQ on the PCB. This pin is used to inform SDRAM device that it is being configured for Mirrored mode vs. Standard mode. With the MIR pin connected to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSS if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1), CA4 with CA5 (not CA3).

To place two DDR5 SDRAMs on the same X-Y location of top and bottom and set the MIR pin VSS/VDDQ will reduce the distance between the same number CA, and reduce the stub trace length.

Note that the CA[13] function is only relevant for certain densities (including stacking) of DRAM component. In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected to VDDQ.

If MIR is employed, the CA12 pin of DRAM (which is now changed to CA13 by MIR) needs to be tied to VDDQ.

The MIR pin configuration is documented in the Checklist which is zipped with the reference design, [and the Annex Specification will identify how MIR is used.](#)

8.5 DIMM Routing Space Constraints

These design rules are intended to be used for the reference DIMM designs submitted to JEDEC for ballot.

When rules which are not defined here are used, it should be noted in the annex for each specific raw card. These rules are for design of the reference card only. It is not required that these rules be met by individual manufacturers building from the reference designs.

DIMMs manufactured from the reference designs may use modified rules to support their manufacturing process.

Table 14 — Routing Space Constraints

	Category	Item	Constraint Value	Note
1	Via	Drill/Pad/Anti-pad/Soldermask	0.20/0.40/0.60/ Soldermask feature may vary depending on designer preference.	One example is setting the soldermask equal to the pad and allowing the PCB shop to adjust as required. Rule may be different between SMD and non-SMD.
2	Spacing	copper to copper (Outer/Inner)	0.075 / 0.070	
3	Spacing	Pad to pad (For pads of different components that are soldered down.)	0.200	
4	Spacing	Line to (N)SMD pad (12 V / the others)	0.113 / 0.100	
5	Spacing	Line to line (Single / Diff pair)	0.100 / 0.090	
6	Spacing	Line to shape	0.125	Where impedance is important, use the 0.20 rule.
7	Spacing	Shape to shape	0.100	
8	Spacing	Via(pad) to NSMD pad (12 V / the others / same Net)	0.113 / 0.100 / 0.100	
9	Spacing	Via(pad) to SMD pad (12 V / the others / same Net)	0.113 / 0.100 / 0.020	
10	Spacing	Via(pad) to Via(pad)	0.125	
11	Spacing	Via(pad) to Line (Outer/Inner)	0.09 / 0.07	
12	Spacing	Drill wall to Board edge (nominal)	0.450	Nominal board edge and drill being centered in pad
13	Comp to Comp	IC to IC (maximum PKG size)	0.250	Inductor is assumed IC. (Maximum PKG size = 4.3 mm)
14	Comp to Comp	IC (max.) to Passive (nominal)	0.250	
15	Comp to Comp	Passive to Passive (nominal PKG size)	0.250	
16	Copper keepout	Board top edge (nom.) to copper	0.250	
17	Keepout DIMM without HS	Top edge of board to Passive (max.) or IC (max.)	0.300	Nominal board edge and package body maximum size criteria
18	Keepout DIMM with HS	Top edge of board to Passive (max.) or IC (max.)	TBD	
19	Keepout SODIMM	lower edge of board to Passive (max.) or IC (max.)	4.200	
20	Keepout U/R/LRDIMM	lower edge of board to Passive (max.) or IC (max.)	4.150	

8.6 DIMM Physical Requirements

8.6.1 Via placement

Signal Vias must not be placed close together (except differential signals) to reduce crosstalk. Recommended to place power or GND Via between Signal Vias.

8.6.2 Component Pad Sizes and Geometry

Pads for components are left to the reference card designer to define. Manufacturers of these SODIMM reference designs may adjust pad sizes and geometry.

8.6.3 Unused CLK, CS Termination

For 1 Rank, Unused CLK should be terminated with two 33 ohm resistors to VDDQ (single ended termination). Unused CS should be terminated with a 39 ohm resistor to VSS.

8.6.4 DQ/CA Stub Resistor

No DQ, Command/address stub resistor for all DDR5 SODIMMs.

8.6.5 ZQ Calibration Wiring

The DDR5 SDRAMs have a ZQ pin. This is intended to calibrate the on-die resistors for the drivers and the terminations. All SODIMMs must connect a $240\ \Omega \pm 1\%$ resistor from this pin of the SDRAM to ground (VSS). Every SDRAM package must have its own ZQ resistor. Sharing is not allowed.

8.6.6 TEN Wiring

TEN is a test enable pin on the SDRAMs. It is not intended to be used on SODIMM modules. It must be tied low VSS at each SDRAM.

8.6.7 Loop Back Wiring

DDR5 SODIMM modules do not have Loopback signal connectivity to the edge connector pins. However, Loopback functionality is useful for module debug, so at the initial design Loop Back signals are connected to the test pads on the modules. The topology should be a daisy chain. The test pads are required for each channels A and B. On the production designs, test pads can be removed.

8.6.8 MIR Wiring

With the MIR pin connected to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSSQ if no CA mirror is required.

The MIR pin connection information may be found in each Reference Design package.

8.6.9 CA_ODT Wiring

For the DDR5 SODIMM, usually only the DRAMs at the end of fly-by connected to VDDQ. The CA_ODT pin connection information may be found in each Reference Design package.

8.6.10 CAI Wiring

With the CAI pin connected to VDDQ, DRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSS if no CA inversion is required. Usually, DDR5 SODIMMs do not need the inversion. The CAI pin cannot be left floating, it must be connected to VSS on the DDR5 SODIMM.

8.7 Reference Stackups

The clause defines the preferred stackup for 8 and 10 layer SODIMMs. Stackup for specific cards may be different from the preferred stackup in the tables below.

Multiple factors influence module stackup definition, and it is expected that module vendors will define their stackups in conjunction with PCB vendors, based on many factors including; material properties, material availability, electrical performance, and cost. The stackups shown here are intended for reference only, in order to demonstrate feasibility of the key performance.

The actual layer construction, trace widths and target impedances used for the design and simulation are documented in each annex.

Table 15 — Preferred 10 Layer Stackup for SO-DIMMs

Layers				
	Solder Mask	15 μ m		
1	Cu	45 μ m	Signal	3/8 oz + Plating
	Prepreg	70 μ m		
2	Cu	15 μ m	VDD/VSS	1/2 oz
	Core	180 μ m		
3	Cu	15 μ m	Signal	1/2 oz
	Prepreg	70 μ m		
4	Cu	15 μ m	VDD/VSS	1/2 oz
	Core	70 μ m		
5	Cu	15 μ m	Signal	1/2 oz
	Prepreg	180 μ m		
6	Cu	15 μ m	Signal	1/2 oz
	Core	70 μ m		
7	Cu	15 μ m	VDD/VSS	1/2 oz
	Prepreg	70 μ m		
8	Cu	15 μ m	Signal	1/2 oz
	Core	180 μ m		
9	Cu	15 μ m	VDD/VSS	1/2 oz
	Prepreg	70 μ m		
10	Cu	45 μ m	Signal	3/8 oz + Plating
	Solder Mask	15 μ m		

NOTE 1 Total thickness 1200 \pm 100 μ m as measured across connector contact fingers (without solder mask).

8.7 Reference Stackups (cont'd)

Table 16 — Preferred 8 Layer Stackup for SODIMMs

Layers				
	Solder Mask	15 μ m		
1	Cu	45 μ m	Signal	3/8 oz + Plating
	Prepreg	70 μ m		
2	Cu	15 μ m	VDD/VSS	1/2 oz
	Core	65 μ m		
3	Cu	15 μ m	Signal	1/2 oz
	Prepreg	330 μ m		
4	Cu	15 μ m	VDD/VSS	1/2 oz
	Core	65 μ m		
5	Cu	15 μ m	Signal	1/2 oz
	Prepreg	330 μ m		
6	Cu	15 μ m	Signal	1/2 oz
	Core	65 μ m		
7	Cu	15 μ m	VDD/VSS	1/2 oz
	Prepreg	70 μ m		
8	Cu	45 μ m	Signal	3/8 oz + Plating
	Solder Mask	15 μ m		

NOTE 1 Total thickness 1200 \pm 100 μ m as measured across connector contact fingers (without solder mask)

8.8 Impedance Targets

The impedances defined here are the design targets.

Three impedances are defined for DDR5 SODIMMs.

1. 55 $\Omega \pm 10\%$ (typically achieved with 0.075 mm trace widths)
2. 40 $\Omega \pm 10\%$ (typically achieved with 0.15 mm trace widths)
3. 30 $\Omega \pm 10\%$ (typically achieved with 0.20 mm trace widths)

The differential traces are routed with the single ended traces defined above with 0.10 mm space.

The typical differential impedances are below.

1. Single 40 Ω (0.15 mm) trace widths with a 0.10 mm space: typically 70 Ω
2. Single 30 Ω (0.20 mm) trace widths with a 0.10 mm space: typically 54 Ω

They are the result of the single ended impedance with the spacing, and is not a requirement.

8.8 Impedance Targets (cont'd)

Table 17 — Target Impedance Assignment by Signal Type

Signal Type	
CLOCK	30 Ω Single ended with 0.10 mm space (typically 54 Ω differential)
Command /Address	Lead-in: 40 Ω , Loaded: 55 Ω
Chip Select	Lead-in: 40 Ω , Loaded: 55 Ω
DQ	40 Ω
DQS	40 Ω Single ended with 0.10 mm space (typically 70 Ω differential)

8.9 Module Sideband Bus

Please refer to the latest version of the JESD403-1: JEDEC Module Sideband Bus (Sideband Bus).

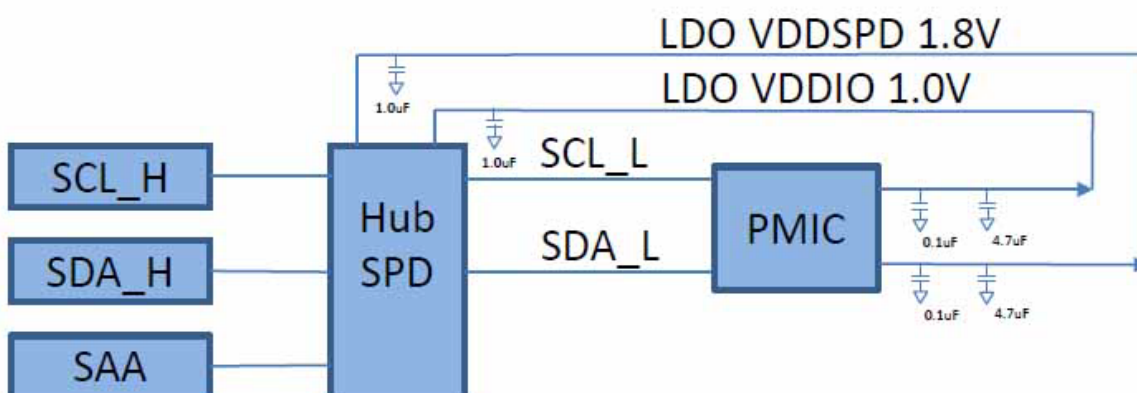


Figure 7 — Sideband Bus Wiring Example

8.10 Bit Swizzling Rules

Unlike DDR4 modules, DDR5 modules do not need to record DQ mapping in SPD, but need to follow the following bit swizzling rules.

- Rule 1: Bits within a nibble + strobe pair must stay together
- Rule 2: Nibbles maybe swapped within the same byte
- Rule 3: Definition of mapping is for rank 0 only. All even ranks have the same DQ mapping.

Even rank to odd rank mapping is to swap bit 0 with bit 1, swap bit 2 with bit 3, swap bit 4 with bit 5, and swap bit 6 with bit 7

The DDR5 SODIMM design should follow the DQ mapping of the JEDEC Reference SODIMM Design of the same configuration. For example, newly designed 1Rx16 SODIMM should follow the DQ mapping of approved 1Rx16 JEDEC DDR5 SODIMM Reference design.

9 DIMM Impedance Profile

DIMM impedance Profile is documented in each Annex.

10 Serial Presence Detect Component Specifications

Please refer to the latest version of JESD400-5: DDR5 Serial Presence Detect (SPD) Contents

11 Product Label

Please refer to the latest version of JESD401-5: DDR5 DIMM Label.

12 JEDEC Process

JEDEC provides PCB reference designs for DIMM modules. The designs are divided into families, one of which is Small Outline DIMMs (SODIMMs). Letters (A, B, C, etc.) are used to define specific configurations (raw cards) of modules such as 2 rank with x8 based SDRAMs. Additional characteristics may further refine cards into specific raw card (R/C) letters. Letter assignments are arbitrary and usually chronological. There is no other association to the letter assignments.

R/Cs are reviewed and balloted by JEDEC members before being placed on the JEDEC website as reference designs. This is called registration. The initial registration is 0. A specific card may be the registration of R/C A0. Subsequent design updates to the reference design go through the same balloting process and increment the registration number from 0 to 1 or the next highest number.



Standard Improvement Form**JEDEC Standard No. JESD309**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by

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